ExTc - VII
AMS VL61

4/6/18

Q. P. Code : 50896

(3 Hours) (Total Marks : 80)

N.B: (1) **Question No.1 is compulsory.**
(2) Solve **any three** questions from the remaining **five.**
(3) **Figures** to the **right** indicate **full marks.**
(4) Assume suitable **data** if **required** and **mention the same in the answer sheet.**

1 Solve **any four** : **20**

(a) What are performance parameters of current source/sink? How to improve the same.

(b) For the circuit shown in Fig 1a find gain of amplifier if $(W/L)_1=50$, $(W/L)_2=10$, $\mu n/\mu p=3$, $I_1=0.75Is$.

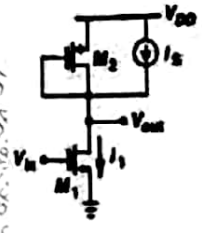

Fig 1a

(c) Explain various types of errors associated with sample and hold circuit.

(d) Explain the effect of Vin, CM on Drain Currents of M1 and M2, Vp, and Vout1 & Vout2 with respect to differential amplifier shown in Fig 1d

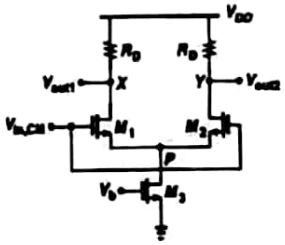

Fig 1d

(e) In resistive load common source amplifier $R_D=1.5K$, $V_{DD}=5V$, $V_{TH}=1V$, $unCox=100uA/V^2$ Find size of transistor if required gain is 4.

2 (a) Explain the various trades - off in analog design with the help of Analog Octagon. **10**

(b) Derive expression voltage gain of saturated load NMOS common source amplifier and show that its gain is independent of bias currents **10**

3 (a) Explain in detail working of switched capacitor Differentiator with neat circuit diagram and appropriate waveforms. **10**

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(b) Small-signal differential voltage gain Av>100V/V, higher cut-off frequency f_{3dB} = 100KHz, Slew Rate SR ≥ 10V/μS, C_L = 5pF, Input common Mode Range (ICMR = −1.5V to 2V, Power Dissipation P_{diss} ≤ 1mW, V_{DD} = 2.5V, V_{SS} = −2.5V. Use transistors with V_{TN} = 0.7V, μnCox = 110μA/V², λ_n = 0.04V⁻¹, V_{TP} = −0.7V, μpCox = 50μA/V², λ_p=0.05V⁻¹ 10

Design current mirror load differential amplifier to meet the following specifications)

4 (a) Explain with the help of neat diagram working of CMOS band gap reference generator and derive the expression for its output voltage. 10

(b) Explain in detail working of charge scaling DAC? What are the limitation of charge scaling DAC and how to overcome the same? 10

5 (a) Explain working of successive Approximation Register (SAR) ADC 10

(b) Consider 4-bit DAC with following measured output voltage with V_{REF} = 5V. Find DNL and INL. Does this DAC provide 4-bit resolution? 10

{0.00:0.3191:0.625:1.1375:1.025:1.5625:1.755:2.1875:2.5:2.8125:3.125:3.5175:3.75:4.0625:4.495:4.7875}

6 Write short notes on **any four** 20

(a) Mixed Signal layout issues

(b) Cyclic ADC

(c) MOSFET as sampling switch

(d) OpAmp Compensation techniques

(e) DAC Specifications